floating gate [therefrom] by [a] said second insulation layer, at least a portion of said control gate being disposed over a portion of said substrate and being separated therefrom by said second insulating layer;

an erase gate [generally placed on a second side] formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated [therefrom] from said second one of said side walls by said second insulation layer;

a drain region formed in a portion of said substrate proximate said control gate [generally disposed on a first side of said floating gate]; and

a source region [generally disposed on a second side of said floating gate] formed in a portion of said substrate proximate said erase gate.

8. (Once Amended) A memory array disposed on a substrate comprising a plurality of memory cells each having a floating gate separated from said substrate by a first insulating layer, an erase gate, a control gate separated from said floating gate by a second insulating layer, a source region, and a drain region, comprising:

a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same row are connected by a common word-line, the erase gates of the memory cells in the same rows are connected by a common erase line, [and] the source regions of the memory cells in the same rows are connected by a common source line, and the drain regions of memory cells in the same columns are commonly connected via a common drain line, wherein at least a portion of each said control gate is disposed over a portion of said substrate and separated therefrom by said second insulating layer; and

control circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array.

16. (New) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;